AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

- 1. (withdrawn-currently amended) A transistor for active matrix display comprising a microcrystalline silicon film [[(5)]] and an insulator [[(3)]], the crystalline fraction being above 80%, wherein it comprises a plasma treated interface [[(4)]] located between the insulator [[(3)]] and the microcrystalline silicon film [[(5)]] so that the said transistor [[(1)]] has a linear mobility equal or superior to 1.5 cm2Wls~1, shows threshold voltage stability and wherein the microcrystalline silicon film [[(5)]] comprises grains [[(6)]] whose size ranges between 10 nm and 400 nm.
- 2. (withdrawn) A transistor for active matrix display according to claim 1, wherein said grain size ranges between 100 $\,$ nm and 200 $\,$ nm.
- 3. (withdrawn-currently amended) A transistor for active matrix display according to claim 1, wherein the microcrystalline silicon film [[(5)]] thickness is comprised between 100 nm and 450 nm.

- 4. (withdrawn-currently amended) A transistor for active matrix display according to claim 1, wherein said transistor [[(1)]] has a top-gate electrode.
- 5. (withdrawn-currently amended) A transistor for active matrix display according to claim 1 wherein said transistor [[(1)]] has a bottom-gate electrode.
- 6. (withdrawn-currently amended) A display unit having a line-column matrix of pixels that are actively addressed, wherein each pixel comprises at least a transistor [[(1)]] according to claim 1.
- (withdrawn) A display unit according to claim 6, wherein said pixels comprise light emissive organic materials.
- (withdrawn) A display unit according to claim 6, wherein said pixels comprise liquid crystals.
- (withdrawn) A display unit according to claim 6, wherein said pixels comprise light emissive polymer materials.
- 10. (withdrawn) A display unit according to claim 6, wherein electronic control means to drive each pixel are at least

partially integrated on the corresponding microcrystalline silicon film.

11. (currently amended) A method for producing a transistor for active matrix display comprising the steps of:

forming an active material and electrodes <u>on a substrate</u>, said active material being formed using <u>a</u> vapor deposition methods method; and said transistor comprising

 $\underline{\text{forming}} \text{ an insulator } \underline{\text{on top of said active material and}}$ electrodes, wherein,

a plasma treated interface is formed on top of said insulator, [[and]]

a microcrystalline film is formed on top of said treated interface at a temperature comprised between 100 and 400°C using at least a deposition chemical element and a crystallisation chemical element wherein [[the]] said microcrystalline silicon film comprises a crystalline fraction being of above 80% and said microcrystalline silicon film comprises grains of a size between 10 nm and 400 nm, and

 $\frac{\text{said plasma treated interface is selected from the}}{\text{group consisting of a SiN_x layer, a SiN_xO_y layer, a SiO_2 layer and glass, and}$

plasma treated interface is formed using a gas selected from the group consisting of N_{2} , N_{2} 0, N_{2} 0 and N_{1} 3.

12-13. (cancelled)

- 14. (previously presented) The method for producing a transistor according to claim 11, wherein the microcrystalline silicon film is formed using a buffer gas selected from the group consisting of Ar, Xe, Kr and He.
- 15. (currently amended) The method for producing a transistor according to claim 11, wherein said crystallisation chemical elements is [[H2]] $\rm H_2$.
- 16. (currently amended) The method for producing a transistor according to claim 11, wherein said deposition chemical elements are selected from the group consisting of $\underline{\text{SiH}_4}$ and $\underline{\text{SiF}_4}$ estated from the group consisting of $\underline{\text{SiH}_4}$ and $\underline{\text{SiF}_4}$ estated from the group consisting of $\underline{\text{SiH}_4}$ and $\underline{\text{SiF}_4}$ estated from the group consisting of $\underline{\text{SiH}_4}$ and $\underline{\text{SiF}_4}$.
- 17. (currently amended) The method for producing a transistor according to claim 11, wherein said deposition chemical elements generate a flux and said crystallisation chemical elements generate a flux, both of which are at equilibrium during the growth of the microcrystalline silicon film.

18. (currently amended) The method for producing a transistor according to claim 11, wherein $\frac{1}{1}$ a top gate transistor $\frac{1}{1}$ formed.

19. (currently amended) The method for producing a transistor according to claim 18, wherein ene patterns the substrate comprising a metallic layer <u>is patterned</u> to form source and drain electrodes.

20. (withdrawn) A method for producing a transistor according to claim 11, wherein one forms a bottom gate transistor.

21. (withdrawn) A method for producing a transistor according to claim 20, wherein the substrate comprises a gate electrode.

22. (cancelled)

23. (previously presented) The method for producing a transistor according to claim 11, wherein the microcrystalline silicon film thickness is comprised between 100 nm and 450 nm.

- 24. (currently amended) The A method for producing a transistor according to claim 11, wherein the microcrystalline silicon film is produced by \underline{a} hot wire technique.
- 25. (currently amended) The method for producing a transistor according to claim 11, wherein the microscrystalline silicon film is produced by \underline{a} radiofrequency[[,]] glow discharge technique.
- 26. (currently amended) The method for producing a transistor according to claim 11, wherein the vapor deposition methods use a radiofrequency glow discharge technique.
- 27. (previously presented) The method for producing a transistor according to claim 26, wherein the vapor deposition methods uses a 13.56 MHz PECVD reactor.